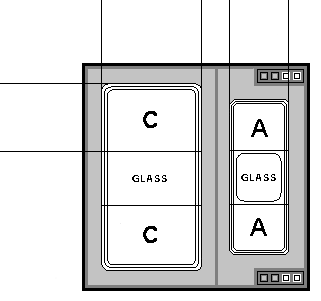
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE & CATHODE ON TOP**

**.028”**

**.028”**



**.011”**

**.005”**

**.007”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: (See above)**

**Backside Potential: CATHODE**

**Mask Ref: ZHO**

**APPROVED BY: DK DIE SIZE .028” X .028” DATE: 8/31/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .010” P/N: 1N821A**

**DG 10.1.2**

#### Rev B, 7/19/02